Notice of Allowability	Application No.	Applicant(s)	
	10/798,063	WANG ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 01/10/2006*.

2. ☒ The allowed claim(s) is/are *5-11 and 15-25*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

A. Claims 5,6,15,18-20,21,22,24, and 25 are allowed over the references of record for the following reasons:

Claim 5 recites, *inter alia*, "etching said oxide layer to form spacers with a first width adjacent to said first gate electrode, spacers having a second width less than said first width adjacent to said second gate electrode, and spacers having a third width." Thus claim 5 requires that all three resultant spacers comprise oxide. Claim 15 recites, "oxide spacers ... formed adjacent to ... gate electrodes in ... first, second, and third transistor regions," as well as a requirement that all three resultant spacers have different net widths. Claim 21 recites, "oxide spacers having a first width ... a second width ... and a third width."

Pfiester 5,021,354 teaches that in CMOS (employing both p-type and n-type) logic circuits, gate electrode spacers of the p-type transistors are advantageously wider than gate electrode spacers of the n-type transistors. Note column 5 lines 8-12 of Pfiester. Ahn 5,874,330 teaches that when logic transistors are placed on the same chips as memory transistors of the same type, it is advantageous to make the gate electrode spacers of the logic transistors wider than the gate electrode spacers of the memory transistors. Note column 3 lines 51-56 of Ahn. For one of skill in the art having these references before himself, it would have

been logical, when placing CMOS and memory on a single chip, to make the gate electrode spacers of the p-type transistors wider than the gate electrode spacers of the n-type transistors and in turn make the gate electrode spacers of the n-type logic transistors wider than gate electrode spacers of the memory transistors. But as Applicant points in his paper or 1/10/06, this combination does not necessarily meet the limitation, found in each of claims 5, 15, and 21, that all three spacers comprise an oxide layer. Because neither Pfiester nor Ahn teach any particular advantages to oxide spacers, a person having skill in the art would have no particular motivation to make all three spacers include oxide.

B. Claims 7-11, 16,17, and 23 are allowed for the reasons set forth in the Paper mailed 10/05/2005.

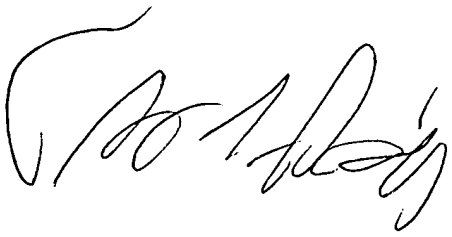
2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
02/06